Updated PLL Test System

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Summarize goals and status of development of new version of PLL test system.

- Reminder of components (see also previous talk in June).
- Survey needs for lab and production testing.
- Short summary of present status.

Components of new system:

New PLL with improvements in several areas:

- Upgraded FPGA to allow continued code development.
- Increased SRAM (16MB in stead of 2MB) to allow module histogramming.
- Addition of programmable XCK generation over range 15-110MHz, and inclusion of FIFO's between present PLL core and output cable to decouple speed of PLL and speed of communication with device under test.
- Addition of support for DTO2 (second serial link from MCC).
- Support of HitBus operation as alternative to digital readout via DTO.
- More NIM outputs for more flexibility (XCK, STR, LV1).

New PCC with minor improvements:

- Support for diagnostic HitBus mode without XCK to device under test.
- Include on-board 14-bit chopper for VCal with settable VLow and VHigh.
- Include support for DTO2 (minor modification to 50-pin connector pinout).
- Include support for temperature measurement with 10K NTC thermistor on module (minor modification to 50-pin connector pinout).

New PICT module (Pixel IC Tester):

- Include PCC core for basic functions.
- Provide direct interface to probe card using new 100-pin MDR connector and shielded flat cable for good high frequency performance.
- Provide fully programmable generation of all output signals (control delay, width, and amplitude) and on all input signals (control delay, width, and threshold) using Pin Drivers and comparators.
- Signals under detailed control are: CMOS inputs (CCK, LD, DI, RSTb), addresses (GA0-GA3), LVDS inputs (XCK, STR, LV1, SYNC), and LVDS output (DO/DTO and DTO2). In addition, provide MCC input (DCI) to support either direct interface to single chips or interface to module via MCC.
- Provide Monitoring functions for all critical voltages and currents. Currents I1-I8 and MonRef are measured as currents across small resistor. Voltages VCCD, VTH, and VCal are measured. Power supplies VDD, VDDA, VCCA are measured using local sense to correct for voltage drops. Currents I(VDD), I(VDDA), I(VCCA) are measured with small series resistor.

Probe Card Adapter:

- Contains minor active circuitry for PICT operation (decoupling, buffers for returning LVDS: MonHit, MonSel, DTO, DTO2, and generation of XCKR).

Production and Lab Testing Configurations

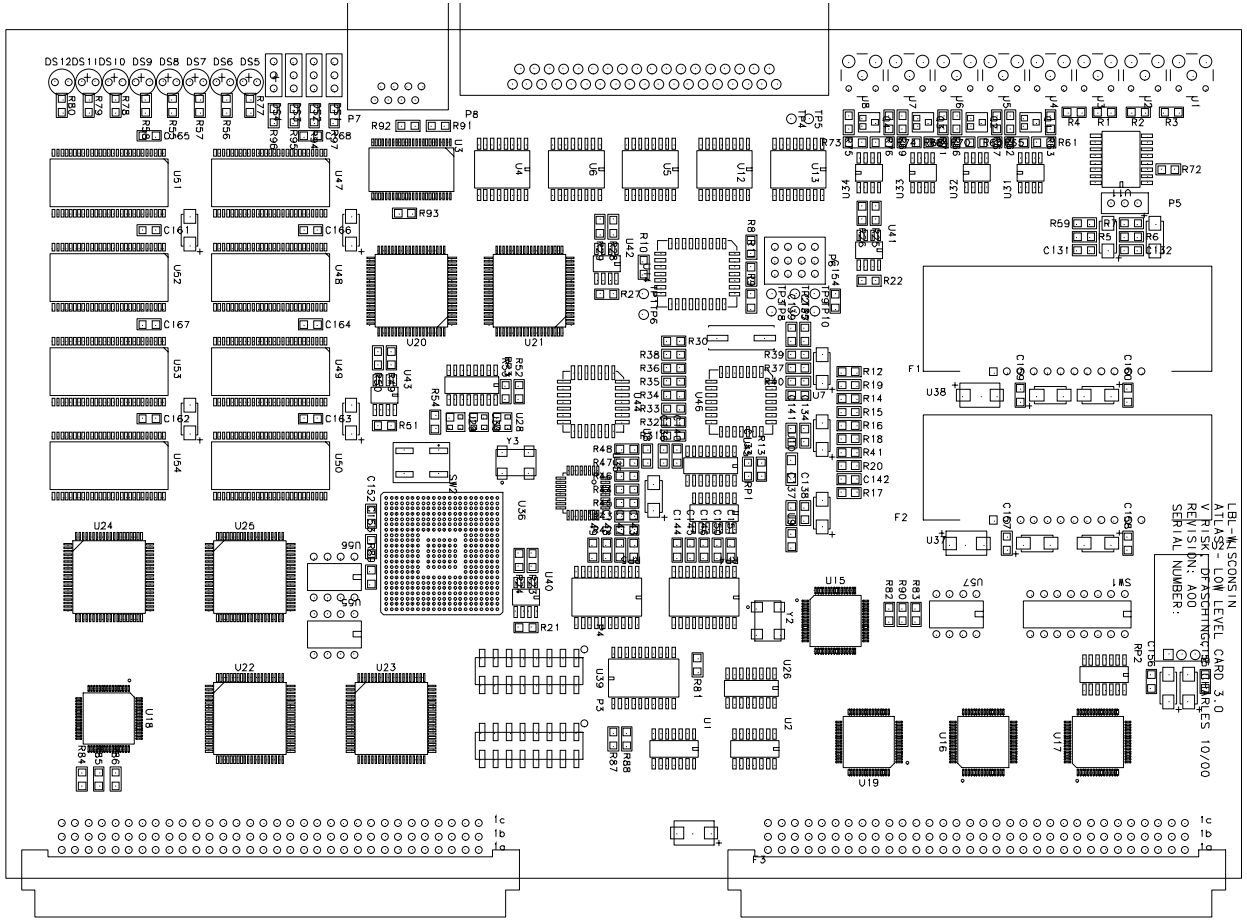
Summarize various configurations needed:

- Design characterization and production Wafer Probing (PLL+PICT+adapter card): In this case, a later generation of probe card could include active components directly. Start with simple adapter card for testing.
- Bare module production probing (PLL+PCC/PICT+special probe card): If we want to interface to the “double probe” concept under development by Milano, need to define mechanism to select which of two chips is sent back to PLL.
- Single chip and module characterization (PLL+PCC+existing support card): Modified 50-pin connector pin assignments are backwards compatible, so this is the present method of operating in the lab and testbeam.
- Production module testing (PLL+PCC/PICT+mini-support card): Have prototyped a new “mini-support” card for this interface.
- Production burn-in testing (PLL + special PCC): The needs for this are not yet well-defined, but system would be based on a PCC core, and including the monitoring capability of PICT. Would nominally support 16 modules, connected using test connector or pigtail connector. Full I/O from only one module would be multiplexed back to PLL for evaluation, but XCK and possibly LV1/VCal would be supplied to all modules.

Status of Components

PLL Status:

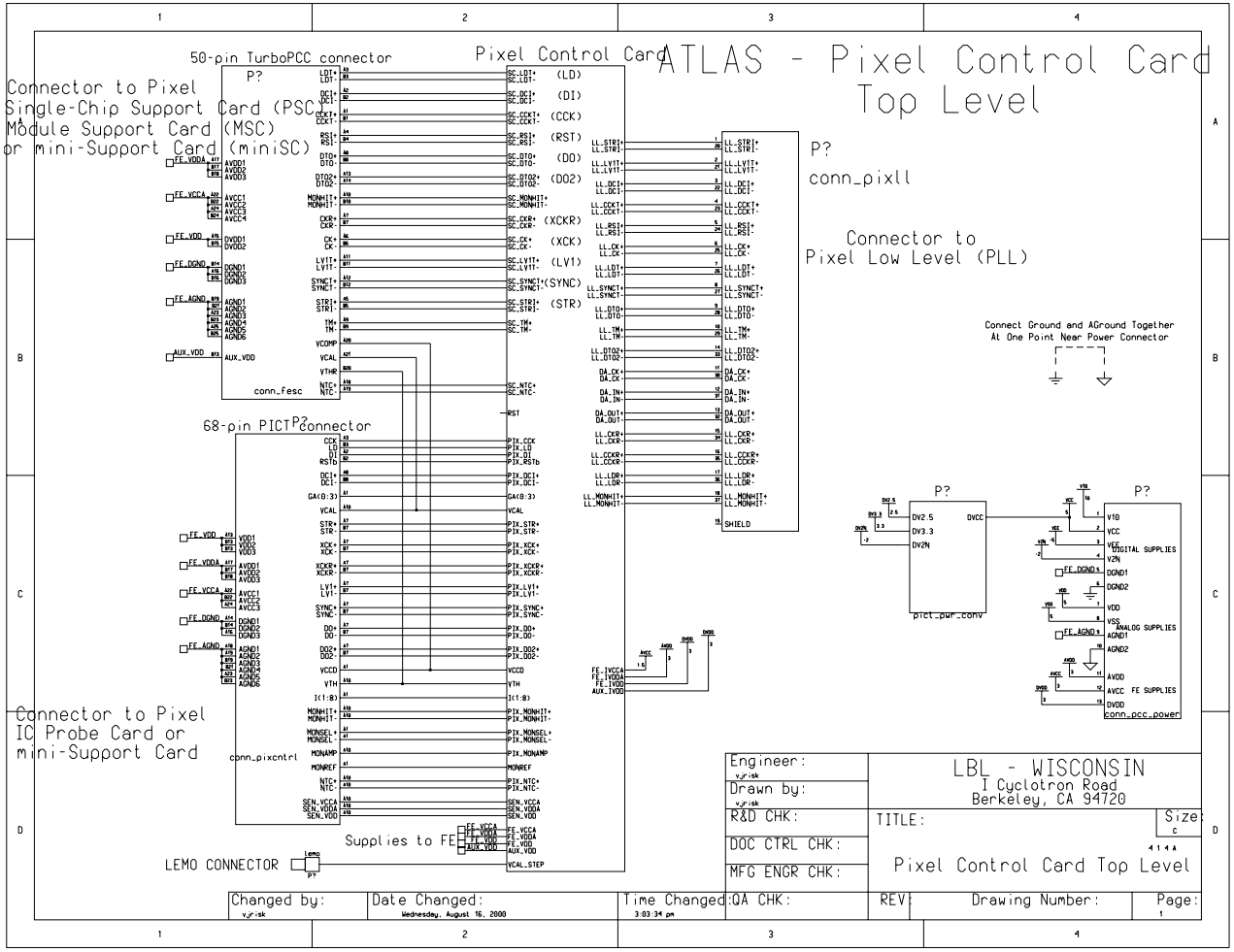
- All components for 10 boards are in hand.
- PC board layout almost complete, should be ready for fab in about 1 week:



- VHDL Upgrades almost complete, but will certainly need debugging...

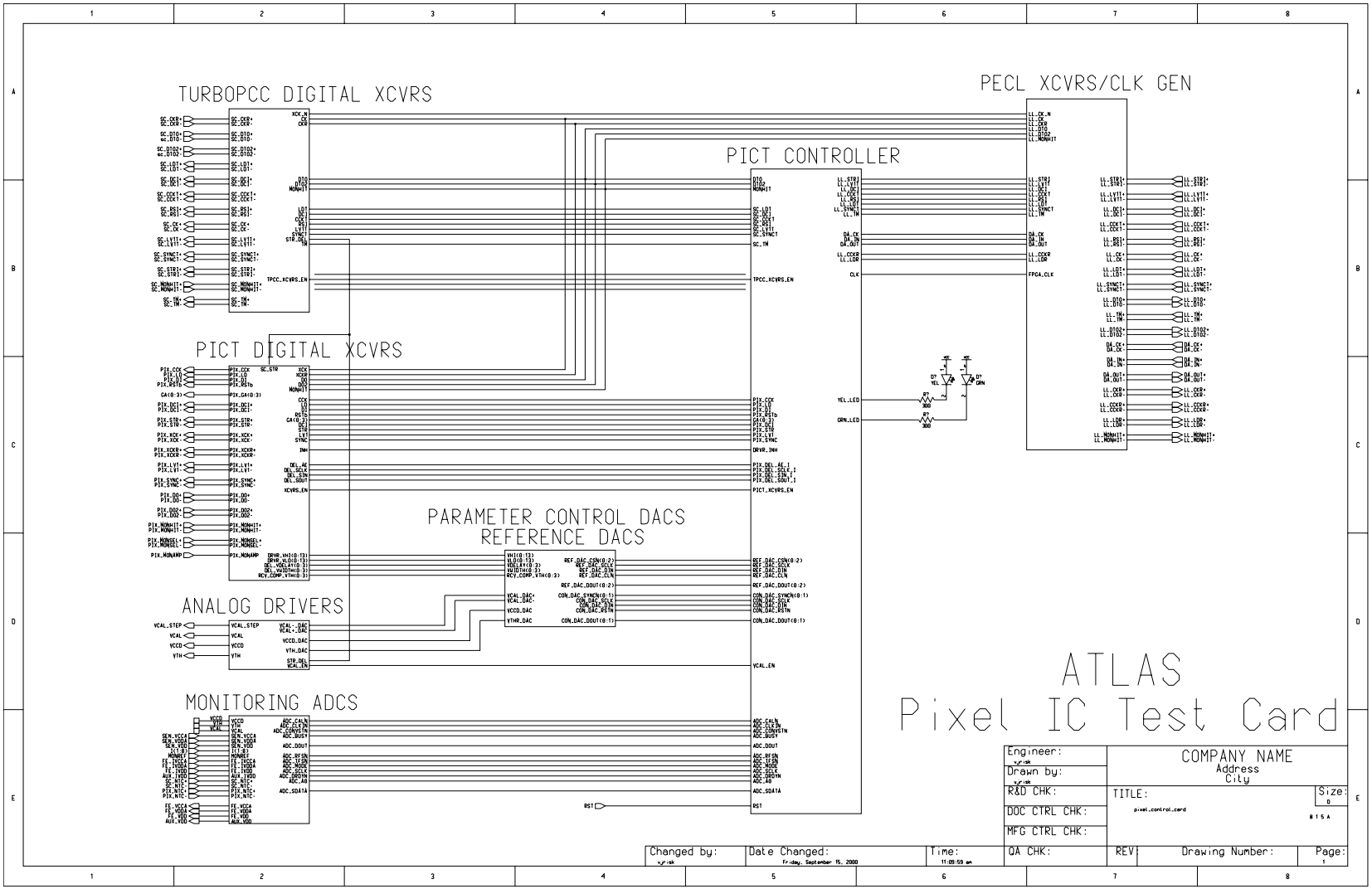
PICT Status:

- Component orders for 5 boards largely completed (worried about long lead times, but we seem to have found all critical components)
- Schematics almost complete, still working on minor details (there are many for this board).



Top level schematic showing core plus three major connectors (PLL, PCC-like, and PICT).

- Not yet clear what board size and mounting arrangement will be. Power on board will be about 40W, and may require modest forced air cooling...



- Cable assembly should fit in standard probe card form factor:

Pleated Foil I/O Cable Assemblies

MDR Version

32

- Mates with standard 3M MDR Boardmount Headers
- Pleated copper foil provides a 360 degree shield
- Supplied as a complete assembly only

Overmolded Assemblies

- Available in 68, 80 and 100 Positions
- Molded-in strain relief
- Can utilize either 4–40 or M2.5 thumbscrews

Metal Shell Assemblies

- Metal shells available in 20, 26, 36, 40, 50, 68, 80 and 100 Positions
- Offer quick release feature for ease of installation
- 68, 80 and 100 positions available with thumbscrews

Low Profile Clam Shell Assemblies

- Available in 68 and 80 Positions
- Overall Height .380 inches

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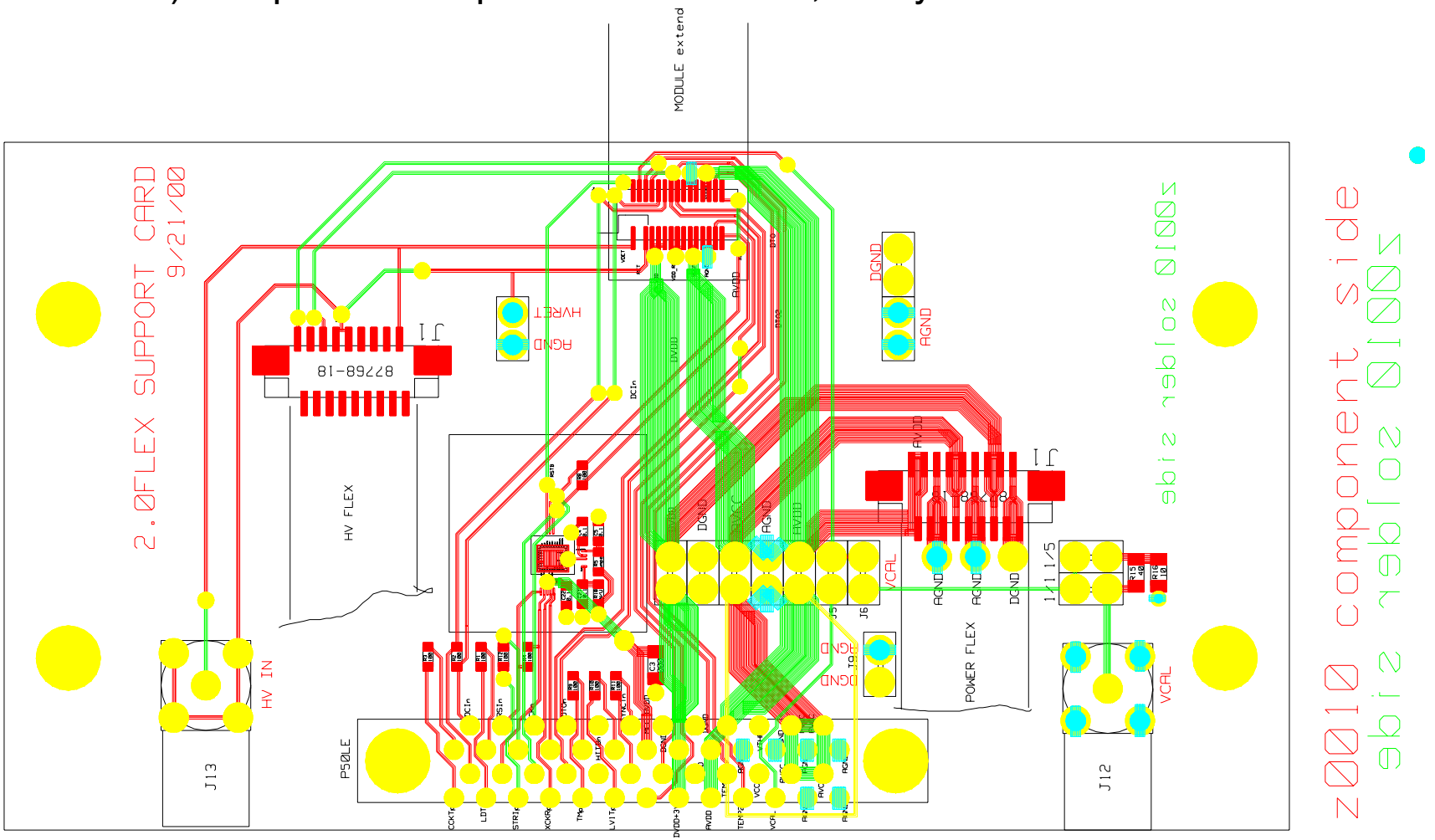
Sheet 1 of 4

- Have already done some SPICE simulations of operation of buffers for LVDS outputs form chip to compare different schemes, but quick “breadboarding” needed to validate performance of fast differential buffers.
- Schematics should be completed in about 2 weeks, and then proceed to board layout, hope to submit for fabrication by end of October at the latest.
- PCC is a subset of PICT schematic at the moment, and so schematics and board layout will follow easily.

Mini-Support Card:

- New card to provide interface between Flex 2.0 modules (using Elco 5087 test connector) and present 50-pin PCC connector, ready to fabricate now:



- Includes Berg connectors to interface to prototype power cables also.